# 3200DX Field Programmable Gate Arrays – The System Logic Integrator™ Family

## Features

### High Capacity

- Up to 40,000 logic gates
- Up to 4 Kbits dual-port SRAM
- Fast wide decode circuitry
- Up to 292 User-programmable I/O Pins

### High Performance

- 200 MHz datapath applications
- 5 ns Dual-Port SRAM
- 100 MHz FIFOs
- 7.5 ns 35-bit Address Decode

### Ease-of-Integration

- JTAG 1149.1 Boundary Scan Testing
- Synthesis-friendly architecture supports ASIC design methodologies
- 95–100% logic utilization using automatic Place and Route Tools
- Deterministic, user-controllable timing via DirectTime™ software tools
- Designer Series™ development tool support including interfaces to popular design environments such as Cadence, Escalade, Exemplar Logic, IST, Mentor Graphics, Synopsys and Viewlogic
- Pin compatible with 1200XL Family

## General Description

The 3200DX, the first device family in Actel's Integrator™ Series, are the first FPGAs optimized for high-speed, high-complexity system logic integration. Based on Actel's proprietary PLICE antifuse technology and state-of-the-art 0.6-micron double metal CMOS process, the 3200DX offers a fine-grained, register-rich architecture with the industry's fastest embedded dual-port SRAM.

The 3200DX was designed to integrate high performance system logic functions typically implemented in multiple CPLDs, PALs, and FPGAs. The 3200DX is the first programmable logic device to embed dual-port SRAM into the programmable array. Offering 5 ns access time, the 3200DX provides the fastest embedded SRAM of any programmable logic device on the market today. This combination of fast, flexible SRAM blocks with a true dual-port architecture, allows designers to implement extremely fast SRAM functions such as FIFOs, LIFOs and scratchpad memory. The large number of storage elements can efficiently address applications requiring wide datapath manipulation and transformation functions such as telecommunications, networking, DSP and bus interfaces. The control and decode functions typically implemented in CPLDs can easily be integrated into the 3200DX by taking advantage of the wide decode modules.

The 3200DX family is supported by Actel's Designer Series 3.0 software which provides a seamless integration into any ASIC design flow. The Designer Series development tools offer automatic or fixed pin assignments, automatic placement and routing (with optional manual placement),

## Product Family Profile

| Device | A3265DX | A32100DX | A32140DX | A32200DX | A32300DX | A32400DX |
|---|---|---|---|---|---|---|
| Capacity | | | | | | |
| Logic Gates | 6,500 | 10,000 | 14,000 | 20,000 | 30,000 | 40,000 |
| Dual-Port SRAM Bits | N/A | 2,048 | N/A | 2,560 | 3,072 | 4,096 |
| Logic Modules | | | | | | |
| Sequential | 510 | 700 | 954 | 1,230 | 1,888 | 2,526 |
| Combinatorial | 475 | 662 | 912 | 1,184 | 1,833 | 2,466 |
| Decode | 20 | 20 | 24 | 24 | 28 | 28 |
| SRAM Modules (64x4 or 32x8) | N/A | 8 | N/A | 10 | 12 | 16 |
| Clocks | 2 | 6 | 2 | 6 | 6 | 6 |
| JTAG | No | Yes | Yes | Yes | Yes | Yes |
| User I/O | 126 | 156 | 176 | 206 | 254 | 292 |

timing analysis, user programming, and debug and diagnostic probe capabilities. In addition, Designer 3.0 provides the DirectTime™ tool which provides deterministic as well as controllable timing. DirectTime allows the designer to specify the performance requirements of individual paths and system clock(s). Using these specifications, the software will automatically optimize the placement and routing of the logic to meet these constraints. Included with Designer 3.0 is Actel's ACTgen™ Macro Builder. ACTgen allows the designer to quickly build fast, efficient logic functions such as counters, adders, FIFOs, and RAM.

The Designer Series tools provide designers the capability to move up to High-Level Description Languages, such as VHDL and Verilog, or use schematic design entry with interfaces to most EDA tools. Designer Series 3.0 is supported on the following development platforms: 386/486 and Pentium PC, Sun, and HP, workstations. The software provides CAE interfaces to Cadence, Escalade, Exemplar Logic, IST, Mentor Graphics, OrCAD, Synopsys, and Viewlogic design environments. Additional development tools are supported through Actel's Industry Alliance Program, including DATA I/O (ABEL FPGA) and MINC.

Actel's FPGAs are an ideal solution for shortening the system design and development cycle and offers a cost-effective alternative for low volume production runs. The 3200DX devices are an excellent choice for integrating logic that is currently implemented in TTL, PALs, CPLDs and FPGAs. Some example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and co-processor functions.

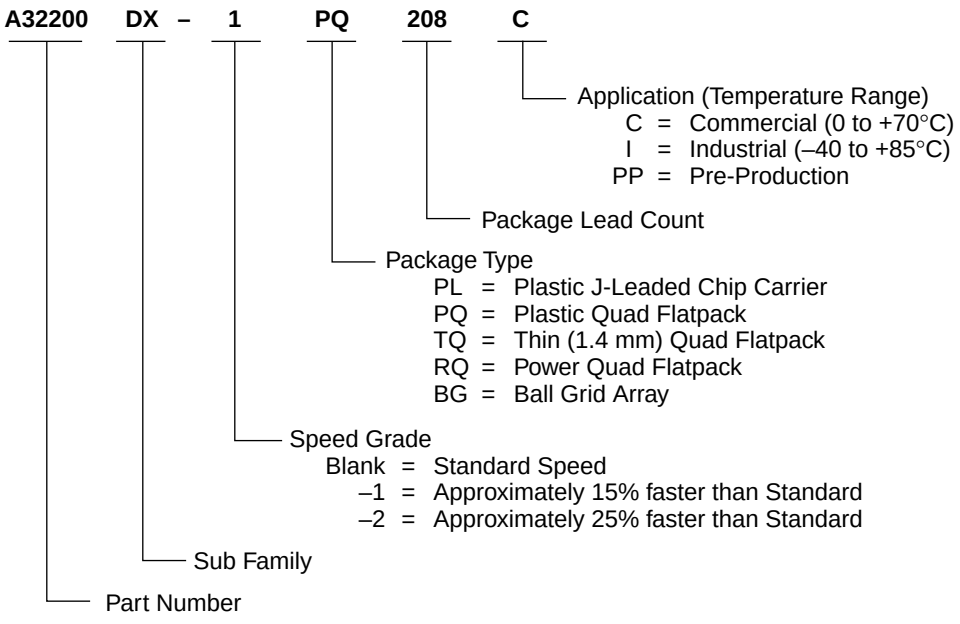
## Device Resources

| Device Series | User I/Os | | | | | | |
|---|---|---|---|---|---|---|---|
| | PLCC 84-pin | PQFP 160-pin | PQFP 208-pin | PQFP 240-pin | TQFP 176-pin | BGA 225-pin | BGA 313-pin |
| A3265DX | 72 | 125 | — | — | 126 | — | — |
| A32100DX | 72 | 125 | 156 | — | 151 | 156 | — |
| A32140DX | — | 125 | 176 | — | 151 | 176 | — |
| A32200DX | — | — | 176 | TBD | — | TBD | 206 |
| A32300DX | — | — | — | TBD | — | — | 254 |
| A32400DX | — | — | — | TBD | — | — | TBD |

***Package Definitions*** *(Consult your local Actel Sales Representative for product availability.)*

*PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, BGA = Ball Grid Array*

## Ordering Information



## Pin Description

CLKA, CLKB Clock A and Clock B (input)

TTL Clock inputs for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground (Input)

Input LOW supply voltage.

I/O Input/Output (Input, Output)

I/O pin functions as an input, output, three-state or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the ALS software.

MODE Mode (Input)

The MODE pin controls the use of multi-function pins (DCLK, PRA, PRB, SDI, TDO). When the MODE pin is HIGH, the special functions are active.

NC No Connection

This pin is not connected to circuitry within the device.

PRA/I/O Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB/I/O Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin’s probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

QCLKA/B,C,D Quadrant Clock (Input/Output)

These four pins are the quadrant clock inputs. When not used as a register control signal, these pins can function as general purpose I/O.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

TCK Test Clock

Clock signal to shift the JTAG data into the device. This pin functions as an I/O when the JTAG fuse is not programmed.

TDI Test Data In

Serial data input for JTAG instructions and data. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed.

TDO Test Data Out

Serial data output for JTAG instructions and test data. This pin functions as an I/O when the JTAG fuse is not programmed.

TMS Test Mode Select

Serial data input for JTAG test mode. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed.

$V_{CC}$ Supply Voltage (Input)

Input HIGH supply voltage.

***Note:*** *TCK, TDI, TDO, TMS are only available on devices containing JTAG circuitry.*

## 3200DX Architectural Overview

The 3200DX family architecture is composed of fine-grained building blocks which produce fast, efficient logic designs. All devices within the 3200DX family are composed of Logic Modules, Routing Resources, Clock Networks, and I/O modules which are the building blocks to design fast logic designs. In addition, a subset of the device family contains embedded dual-port SRAM modules which can implement fast SRAM functions such as FIFOs, LIFOs, and scratchpad memory.

## Logic Modules

The 3200DX contains three types of logic modules: combinatorial (C-modules), sequential (S-modules), and decode (D-modules). Both the C-module and S-module are identical to the 1200XL family logic modules.

The combinatorial module (shown in Figure 1) implements the following function:

Y=!S1*!S0*D00+!S1*S0*D01*S1*!S0*D01+S1*S0*D11

where:

S0=A0*B0

S1=A1 + B1

The S-module is designed to implement high-speed flip-flop functions within a single module. The S-module implements the same logic function as the C-module followed by a sequential block. The sequential block can implement either a D flip-flop or a transparent latch. The S-module can also be configured as fully transparent so that it can be used to implement purely combinatorial logic. The function of the sequential module is determined by the macro selection from the design library. The available S-module implementations are shown in Figure 2.

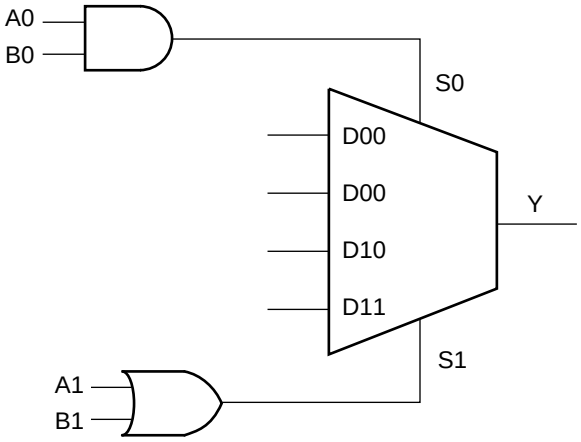



***Figure 1 •*** *C-module Implementation*

D-modules are arranged around the periphery of the device and contain wide decode circuits providing a fast decode function similar to CPLDs and PALs (Figure 3). This is

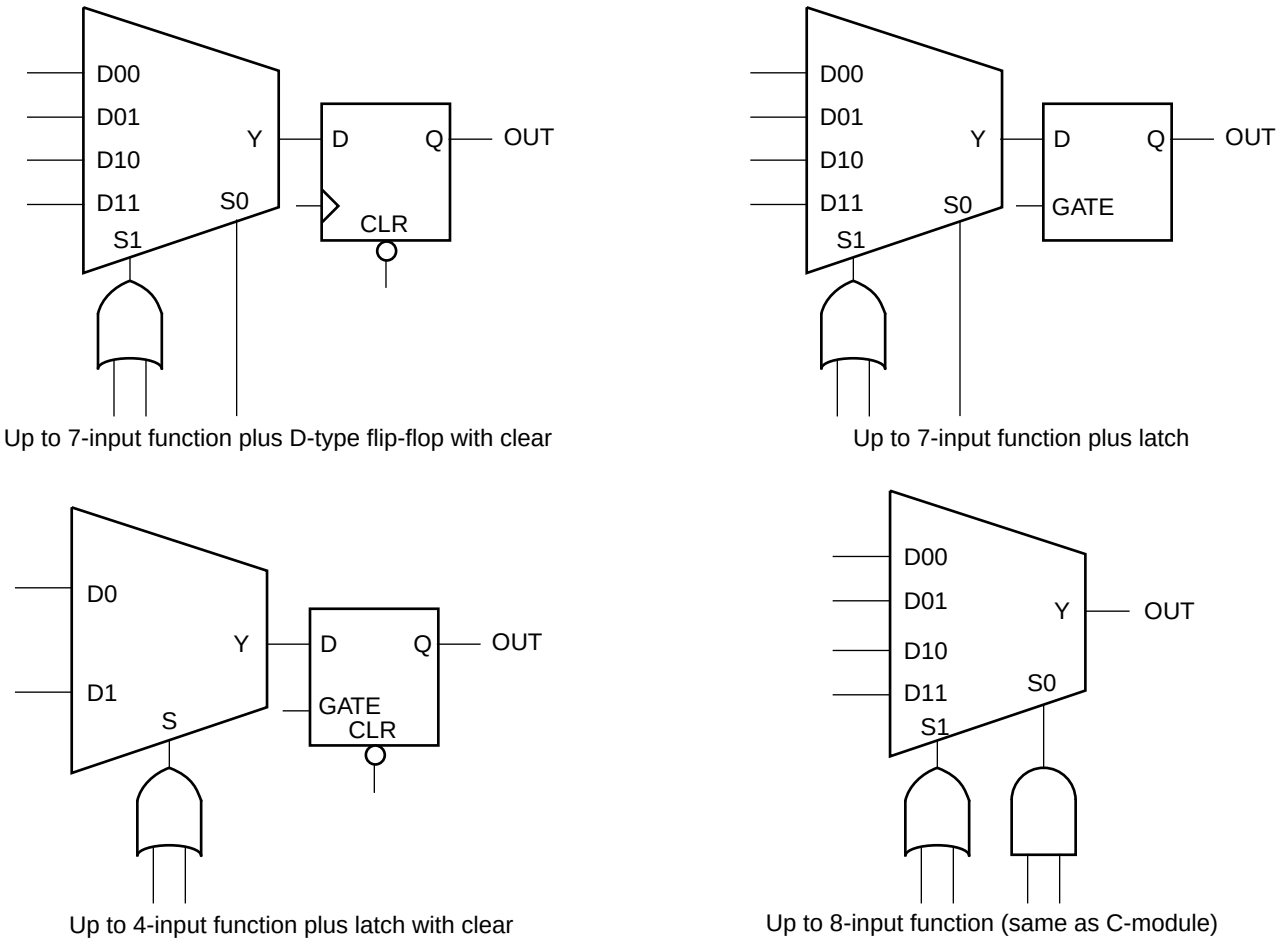



***Figure 2 •*** *S-module Implementations*

analogous to the wide-input AND term in a CPLD or PAL device. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hardwired to an output pin or can be fed back into the array to be incorporated into other logic.

### Dual-Port SRAM Modules

The 3200DX dual-port SRAM modules have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256 bit blocks which can be configured as 32 x 8 or 64 x 4 (refer to Table 1 for the number of SRAM modules within a particular device). The SRAM module block structure allows them to be cascaded together to form user-definable memory spaces. Resources within the 3200DX architecture allow the SRAM modules to be cascaded together without incurring an additional delay penalty. A block diagram of the 3200DX dual-port SRAM block is shown in Figure 4.

The 3200DX SRAM blocks are true dual-port structures containing independent READ and WRITE logic. The SRAM blocks contain six bits of read and write addressing (RDAD[5:0] and WRAD[5:0] respectively) for 64x4 bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM blocks contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The write

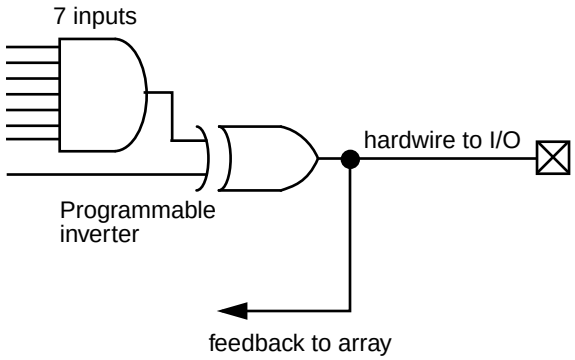



***Figure 3 •*** *D-Module Implementation*

and read ports of the SRAM block have eight data inputs (WD[7:0]) and eight outputs (RD[7:0]). The SRAM block outputs are connected to segmented vertical routing tracks.

The 3200DX dual-port SRAM blocks are ideal for high-speed buffered applications such as DMA controllers and FIFO and LIFO queues. Actel's ACTgen Macro Builder provides the capability to quickly design memory elements, such as FIFOs, LIFOs, and RAM arrays which can be included in any 3200DX design. Additionally, unused SRAM blocks can be used to implement registers for other logic within the design.

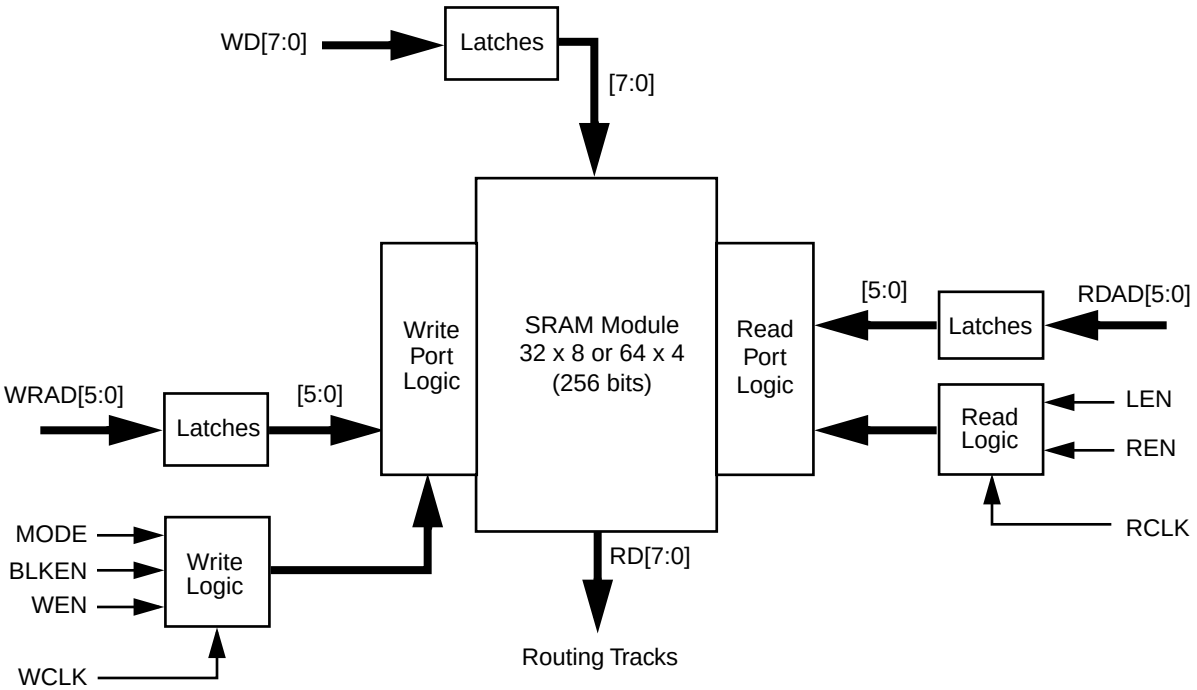



***Figure 4 •*** *Dual-Port SRAM Module*

### I/O Modules

The I/O modules provide the interface between the device pins and the logic array (shown in Figure 5). A variety of I/O configurations, determined by a library macro selection, can be implemented in the module (refer to the Macro Library Guide for more information). I/O modules contain input and output latches as well as a tri-state buffer. These features allow the module to be configured for input, output, or bi-directional pins.

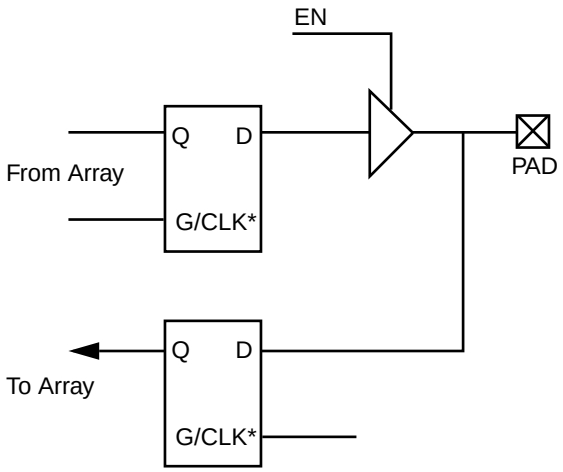



***Figure 5 •*** *I/O Module*

I/O modules contain input and output latches for capturing data prior to and/or from the device pins. In addition, the Actel Designer Series software tools can build a D flip-flop using a C-module in conjunction with the I/O latch to register input and/or output signals. Actel's Designer Series development tools provide a design library of I/O macros which can implement all I/O configurations supported by the 3200DX.

### Routing Structure

The 3200DX architecture uses Horizontal and Vertical routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into pieces called segments. Varying segment lengths allows the interconnect of over 90% of design tracks to occur with only two antifuse connections. Segments can be joined together at the ends, using antifuses, to increase their lengths up to the full length of the track. All interconnects can be accomplished with a maximum of four antifuses.

#### Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 6. Non-dedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

#### Vertical Routing

Other tracks run vertically through the module. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. An example of vertical routing tracks and segments is shown in Figure 6.

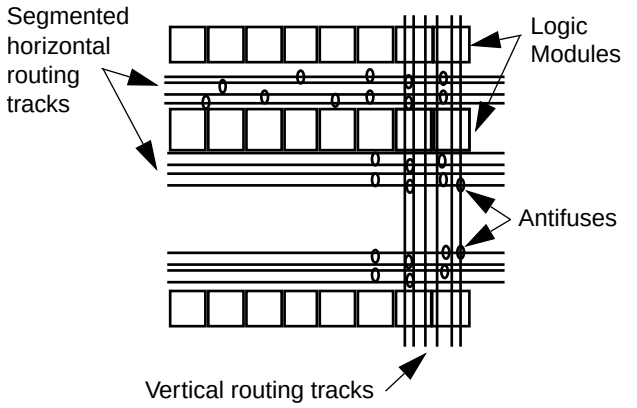



***Figure 6 •*** *Horizontal Routing Tracks and Segments*

#### Antifuse Structures

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a Programmable Logic Device results in highly testable structures as well as efficient programming algorithms. The structure is highly testable because there are no pre-existing connections; therefore, temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

### Clock Networks

Two low-skew, high fanout clock distribution networks are provided in each 3200DX device. These networks are referred to as CLK0 and CLK1. Each network has a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows:

1. Externally from the CLKA pad
2. Externally from the CLKB pad
3. Internally from the CLKINA input
4. Internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

The user controls the clock module by selecting one of two clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. The clock input pads may also be used as normal I/Os, bypassing the clock networks (see Figure 7).

The 3200DX devices which contain SRAM modules (all except A3265DX and A32140DX) have four additional register control resources, called Quadrant Clock Networks (Figure 8). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

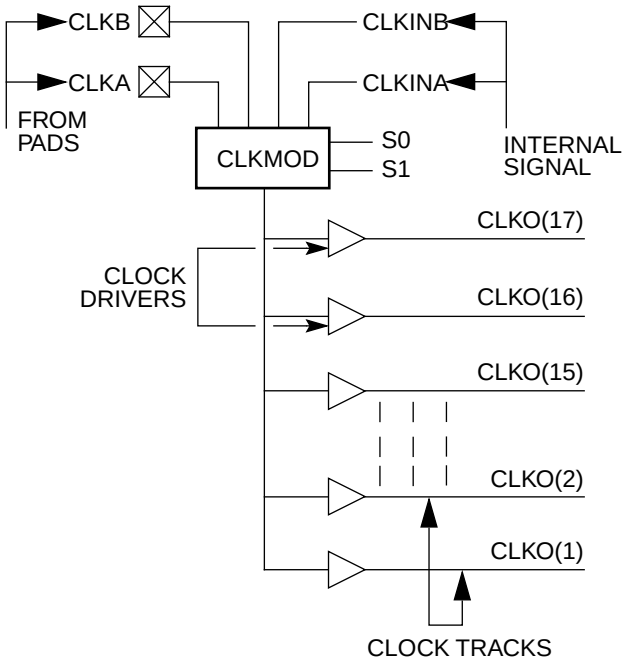
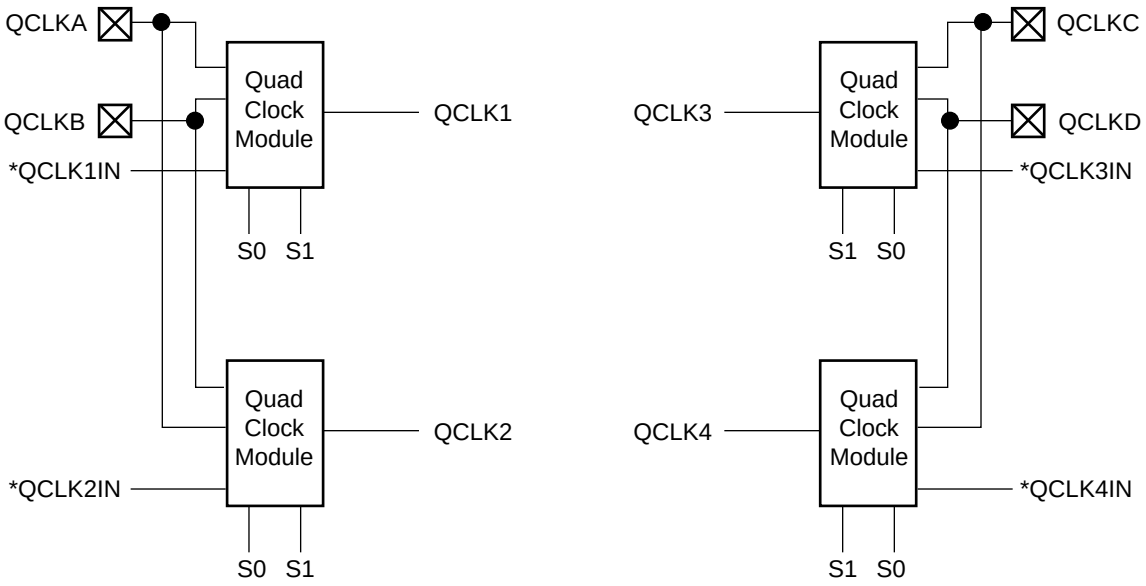



***Figure 7 •*** *Clock Networks*

### Test Circuitry

The 3200DX provides two modes of device and/or board-level testing; JTAG 1149.1 Boundary Scan Testing and Actel's Actionprobe® test facility. Once a 3200DX device has been programmed, the Actionprobe test facility




**QCLK1IN, QCLK2IN, QCLK3IN, and QCKL4IN are internally generated signals.*

***Figure 8 •*** *Quadrant Clock Network*

allows the designer to probe any internal node during device operation to aid in debugging a design.

### JTAG Boundary Scan Testing (BST)

Device pin spacing is decreasing with the advent of fine-pitch packages such as TQFP and BGA packages and manufacturers are routinely implementing surface-mount technology with multi-layer PC boards. Boundary scan is becoming an attractive tool to help systems manufacturers test their PC boards. The Joint Test Action Group (JTAG) developed the IEEE Boundary Scan standard 1149.1 to facilitate board-level testing during manufacturing.

IEEE Standard 1149.1 defines a 4-pin Test Access Port (TAP) interface for testing integrated circuits in a system. The 3200DX family provides four JTAG BST pins: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK) and Test Mode Select (TMS). Devices are configured in a JTAG "chain" where BST data can be transmitted serially between devices via TDO to TDI interconnections. The TMS and TCK signals are shared between all devices in the JTAG chain so that all components operate in the same state.

The 3200DX family implements a subset of the IEEE 1149.1 Boundary Scan Test (BST) instruction in addition to a private instruction to allow the use of Actel's Actionprobe facility with JTAG BST. Refer to the IEEE 1149.1 specification for detailed information regarding JTAG testing.

### JTAG Architecture

The 3200DX's JTAG BST function is enabled by programming the JTAG anti-fuse. When JTAG BST is not enabled, the TMS, TCLK, and TDI pins become user I/O. Otherwise, these three pins are dedicated exclusively to JTAG testing.

The 3200DX JTAG BST circuitry consist of a Test Access Port (TAP) controller, JTAG instruction register, JPROBE register, bypass register and boundary scan register. Figure 9 is a block diagram of the 3200DX JTAG circuitry.

When a device is operating in JTAG BST mode, four I/O pins are used for the TDI, TDO, TMS, and TCK signals. An active reset (nTRST) pin is not supported, however the 3200DX contains power-on reset circuitry which resets the JTAG BST circuitry upon power-up. The following table summarizes the functions of the JTAG BST signals.

| JTAG Signal | Name | Function |
|---|---|---|
| TDI | Test Data In | Serial data input for JTAG instructions and data. Data is shifted in on the rising edge of TCLK. |
| TDO | Test Data Out | Serial data output for JTAG instructions and test data. |
| TMS | Test Mode Select | Serial data input for JTAG test mode. Data is shifted in on the rising edge of TCLK. |
| TCK | Test Clock | Clock signal to shift the JTAG data into the device. |

### JTAG BST Instructions

JTAG BST testing within the 3200DX devices is controlled by a Test Access Port (TAP) state machine. The TAP controller drives the three-bit instruction register, a bypass register, and the boundary scan data registers within the device. The TAP controller uses the TMS signal to control

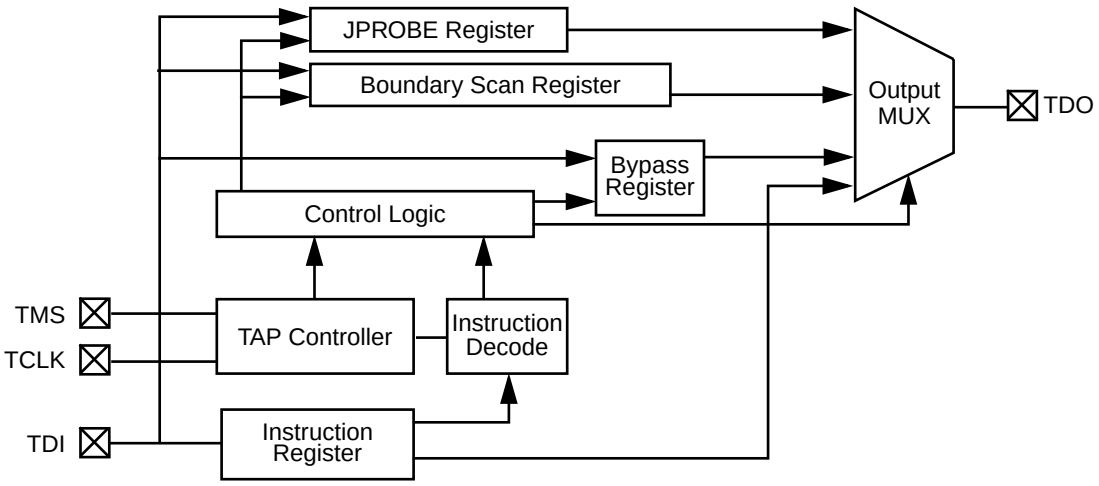



***Figure 9 •*** *JTAG BST Circuitry*

the JTAG testing of the device. The JTAG test mode is determined by the bit stream entered on the TMS pin. The table below describes the JTAG instructions supported by the 3200DX.

| Test Mode | Code | Description |
|---|---|---|
| EXTEST | 000 | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| SAMPLE/ PRELOAD | 001 | Allows a snapshot of the signals at the device pins to be captured and examined during device operation. |
| INTEST | 010 | Refer to IEEE 1149.1 Specification |
| JPROBE | 011 | A private instruction allowing the user to connect Actel's Micro Probe registers to the JTAG chain. |
| USER INSTRUCTION | 100 | Allows the user to build application-specific instructions such as RAM READ and RAM WRITE. |
| HIGH Z | 101 | Refer to IEEE 1149.1 Specification |
| CLAMP | 110 | Refer to IEEE 1149.1 Specification |
| BYPASS | 111 | Enables the by bypass register between the TDI and TDO pins. The test data passes through the selected device to adjacent devices in the JTAG chain. |

### Actionprobe

If a device has been successfully programmed and the security fuse has not been programmed, any internal logic or I/O module output can be observed using the Actionprobe circuitry and the PRA and/or PRB pins. The Actionprobe diagnostic system provides the software and hardware required to perform real-time debugging. Refer to Actel's 1995 Data Book for further information on using the Actionprobe facility.

## Absolute Maximum Ratings[1]

Free air temperature range

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | –0.5 to +7.0 | V |
| $V_I$ | Input Voltage | –0.5 to $V_{CC}$ +0.5 | V |
| $V_O$ | Output Voltage | –0.5 to $V_{CC}$ +0.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |

***Note:***

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*

## Recommended Operating Conditions

| Parameter | Commercial | Industrial | Units |
|---|---|---|---|
| Temperature Range[1] | 0 to +70 | –40 to +85 | °C |
| Power Supply Tolerance | ±5 | ±10 | %$V_{CC}$ |

***Note:***

1. *Ambient temperature ($T_A$) is used for commercial and industrial; case temperature ($T_C$) is used for military.*

## Electrical Specifications

| Symbol | Parameter | | Commercial | | Units |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $V_{OH}$ | HIGH Level Output | $I_{OH}$ = –10 mA (CMOS) | 2.40 | | V |
| | | $I_{OH}$ = –6 mA (TTL) | 3.84 | | V |
| $V_{OL}$ | LOW Level Output | $I_{OL}$ = 10 mA (CMOS) | | 0.50 | V |
| | | $I_{OL}$ = 6 mA (TTL) | | 0.33 | V |
| $V_{IH}$ | HIGH Level Input | | –0.3 | 0.8 | V |
| $V_{IL}$ | LOW Level Input | | 2.0 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Leakage | $V_I$ = $V_{CC}$ or GND | –10 | +10 | µA |
| $I_{CC(S)}$ | Standby $V_{CC}$ Supply Current | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 mA | | 1.5 | mA |
| $I_{CC(D)}$ | Dynamic $V_{CC}$ Supply Current | | | Note 1 | mA |

***Note:***

1. *See "Power Dissipation" section.*

## Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQFP 160-pin package at commercial temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. commercial temp.}}{\theta ja\ (°C/W)} = \frac{150°C - 70°C}{30°C/W} = 2.6W$$

| Package Type | Pin Count | θja | | Maximum Power Dissipation | |
|---|---|---|---|---|---|
| | | Still Air | 300 ft/min | Still Air | 300 ft/min |
| Plastic Quad Flatpack | 160 | 36 °C/W | 30 °C/W | 2.2 W | 2.6 W |
| Plastic Quad Flatpack | 208 | 25 °C/W | 16.2 °C/W | 3.2 W | 4.9 W |
| Plastic Leaded Chip Carrier | 84 | 37 °C/W | 28 °C/W | 2.2 W | 2.9 W |
| Thin Quad Flatpack | 176 | 32 °C/W | 25 °C/W | 2.5 W | 3.2 W |

## General Power Equation

$$P = [I_{CC}standby + I_{CC}active] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$$

Where:

$I_{CC}$standby is the current flowing when no inputs or outputs are changing.

$I_{CC}$active is the current flowing due to CMOS switching.

$I_{OL}$, $I_{OH}$ are TTL sink/source currents.

$V_{OL}$, $V_{OH}$ are TTL level output voltages.

N equals the number of outputs driving TTL loads to $V_{OL}$.

M equals the number of outputs driving TTL loads to $V_{OH}$.

An accurate determination of N and M is problematic because their values depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.

### Static Power Component

Actel FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial, worst case conditions.

| $I_{CC}$ | $V_{CC}$ | Power |
|---|---|---|
| 2 mA | 5.25 V | 10.5 mW |

The static power dissipation by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this number is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

### Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem-pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

### Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1.

$$\text{Power } (\mu W) = C_{EQ} * V_{CC}^2 * F \quad (1)$$

Where:

$C_{EQ}$ is the equivalent capacitance expressed in picofarads (pF).

$V_{CC}$ is power supply in volts (V).

F is the switching frequency in megahertz (MHz).

Equivalent capacitance is calculated by measuring $I_{CCactive}$ at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of $V_{CC}$. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

### $C_{EQ}$ Values for Actel FPGAs

| | |
|---|---|
| Modules ($C_{EQM}$) | 5.2 |
| Input Buffers ($C_{EQI}$) | 11.6 |
| Output Buffers ($C_{EQO}$) | 23.8 |
| Routed Array Clock Buffer Loads ($C_{EQCR}$) | 3.5 |

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piece-wise linear summation over all components.

$$\text{Power} = V_{CC}^2 * [(m \times C_{EQM} * f_m)_{Modules} + (n * C_{EQI} * f_n)_{Inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} \quad (2)$$

Where:

$m$ = Number of logic modules switching at frequency $f_m$

$n$ = Number of input buffers switching at frequency $f_n$

$p$ = Number of output buffers switching at frequency $f_p$

$q_1$ = Number of clock loads on the first routed array clock

$q_2$ = Number of clock loads on the second routed array clock

$r_1$ = Fixed capacitance due to first routed array clock

$r_2$ = Fixed capacitance due to second routed array clock

$C_{EQM}$ = Equivalent capacitance of logic modules in pF

$C_{EQI}$ = Equivalent capacitance of input buffers in pF

$C_{EQO}$ = Equivalent capacitance of output buffers in pF

$C_{EQCR}$ = Equivalent capacitance of routed array clock in pF

$C_L$ = Output load capacitance in pF

$f_m$ = Average logic module switching rate in MHz

$f_n$ = Average input buffer switching rate in MHz

$f_p$ = Average output buffer switching rate in MHz

$f_{q1}$ = Average first routed array clock rate in MHz

$f_{q2}$ = Average second routed array clock rate in MHz

### Fixed Capacitance Values for Actel FPGAs (pF)

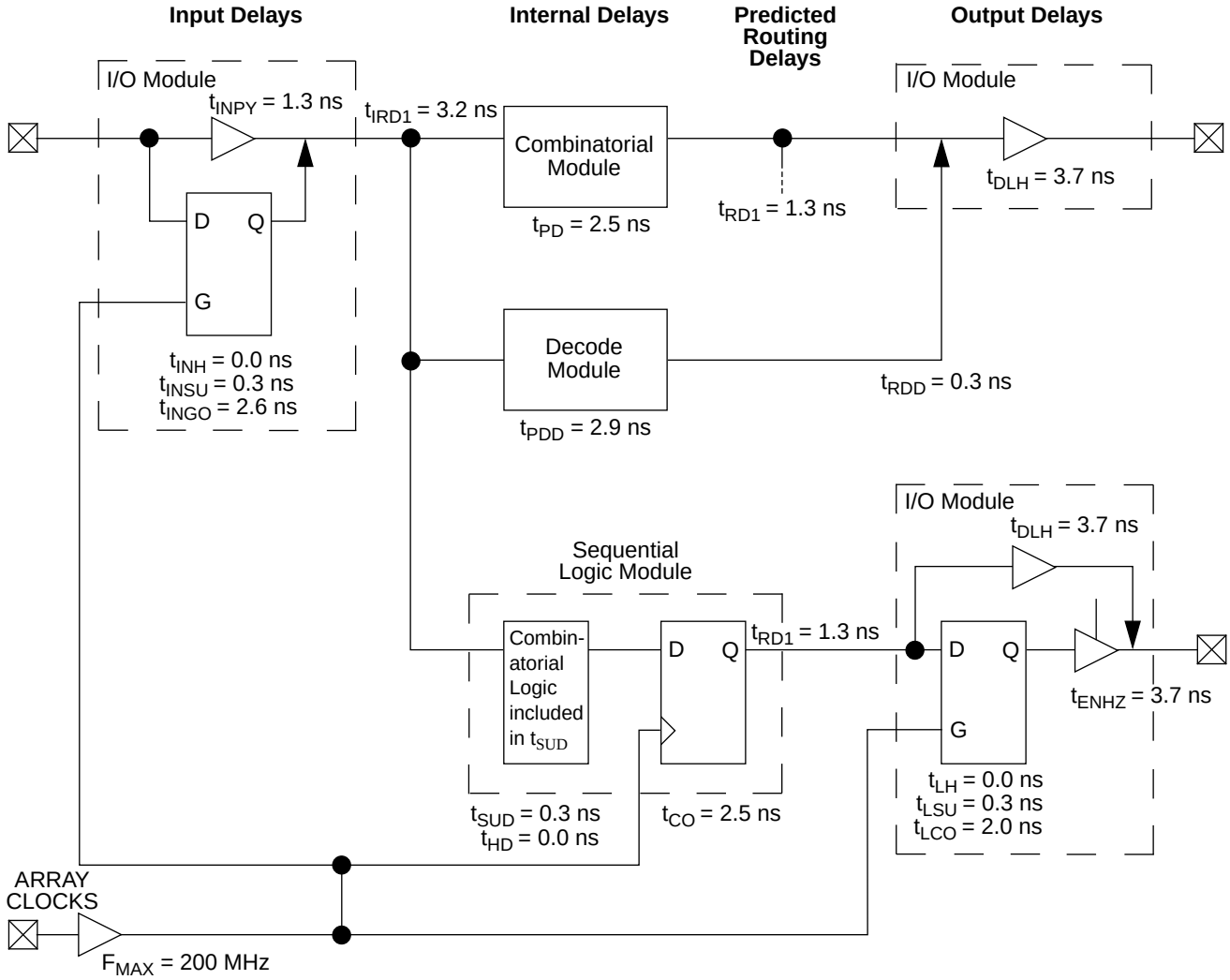
| Device Type | $r_1$ routed_Clk1 | $r_2$ routed_Clk2 |
|---|---|---|
| A3265DX | TBD | TBD |
| A32140DX | TBD | TBD |
| A32200DX | TBD | TBD |

### Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

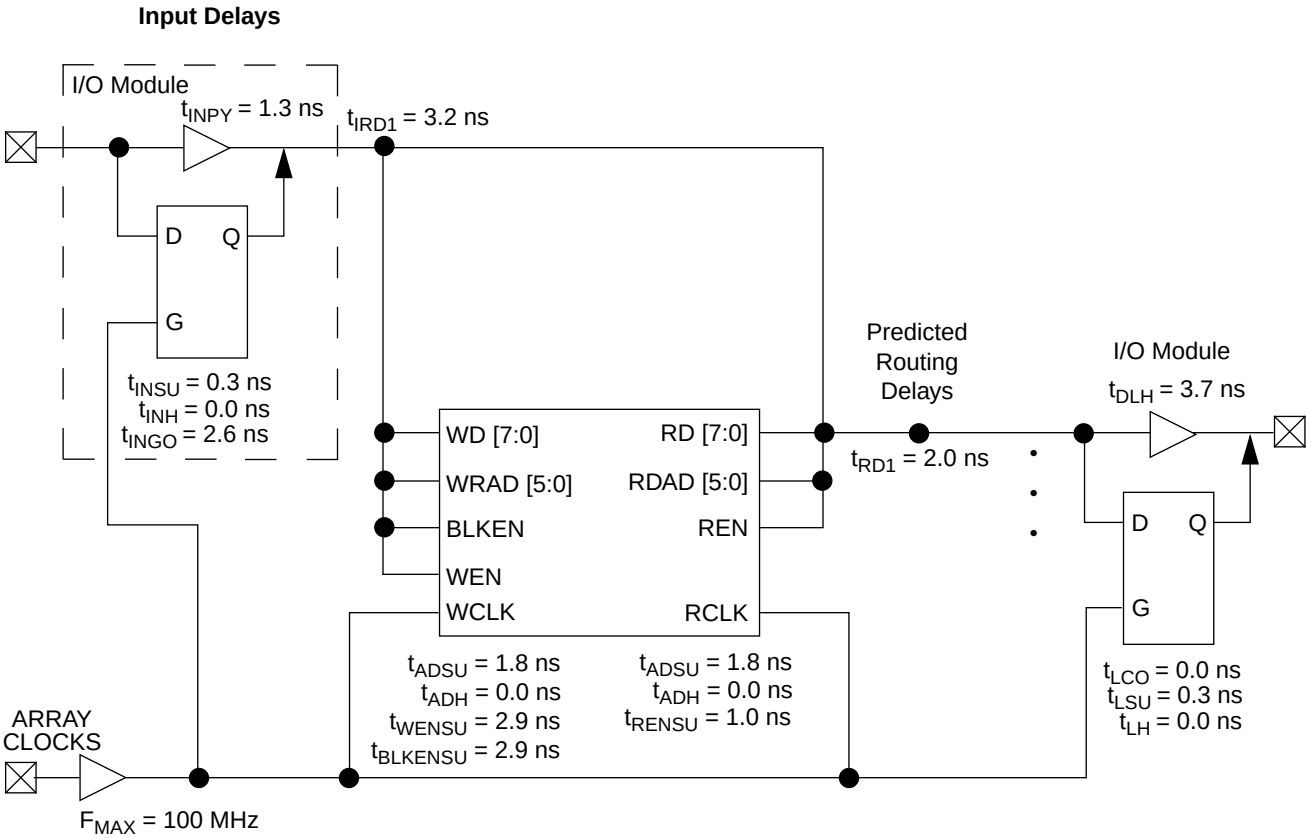
| | |
|---|---|
| Logic Modules (m) | = 80% of combinatorial modules |
| Inputs switching (n) | = # of inputs/4 |
| Outputs switching (p) | = # outputs/4 |
| First routed array clock loads ($q_1$) | = 40% of sequential modules |
| Second routed array clock loads ($q_2$) | = 40% of sequential modules |
| Load capacitance ($C_L$) | = 35 pF |
| Average logic module switching rate ($f_m$) | = F/10 |
| Average input switching rate ($f_n$) | = F/5 |
| Average output switching rate ($f_p$) | = F/10 |
| Average first routed array clock rate ($f_{q1}$) | = F |
| Average second routed array clock rate ($f_{q2}$) | = F/2 |

## 3200DX Timing Model (Logic Functions)*




**Values shown for A3265DX-2 at worst-case commercial conditions.*

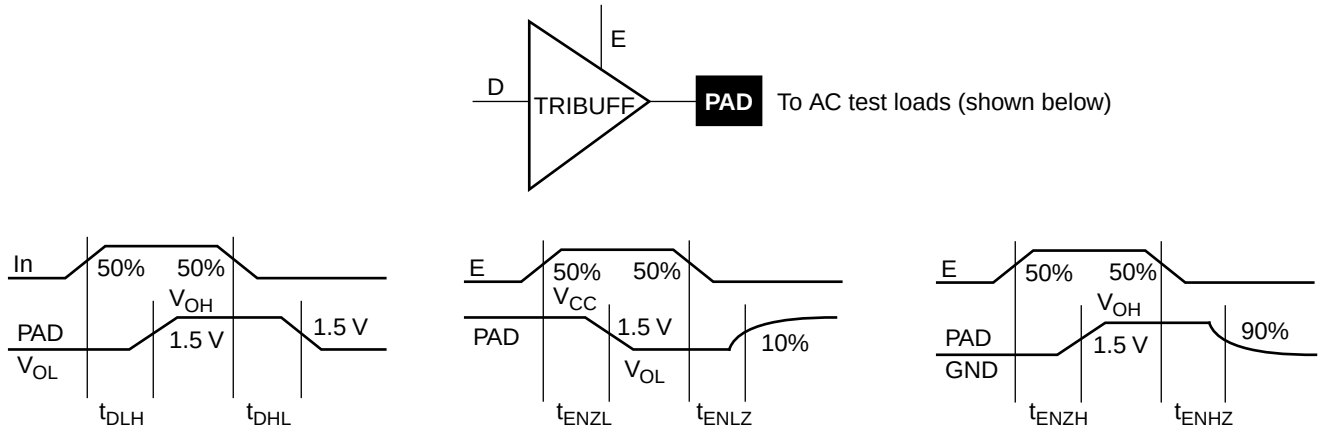
## 3200DX Timing Model (SRAM Functions)*




**Values shown for A32200DX-2 at worst-case commercial conditions.*

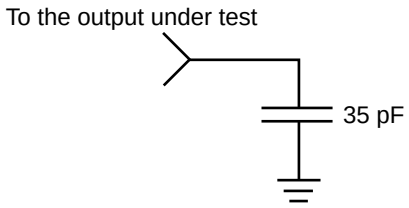
## Parameter Measurement

### Output Buffer Delays

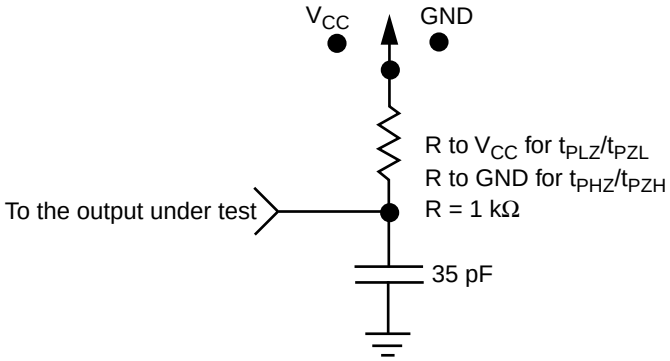



### AC Test Loads

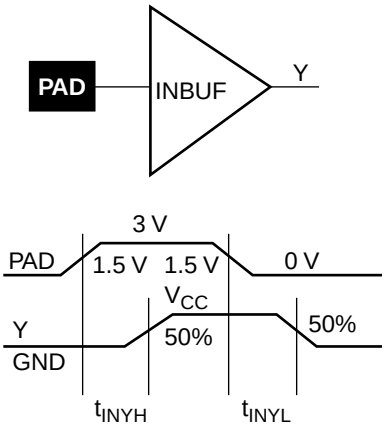
**Load 1**
**(Used to measure propagation delay)**



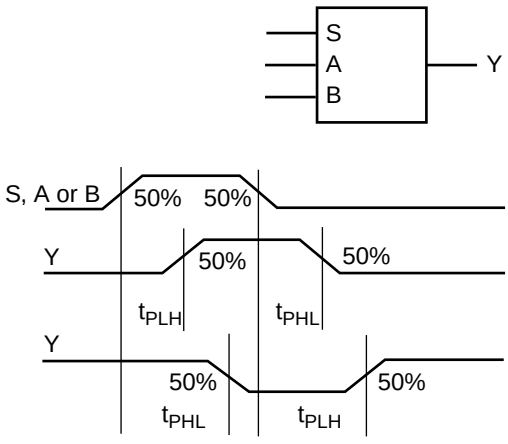

**Load 2**
**(Used to measure rising/falling edges)**




### Input Buffer Delays

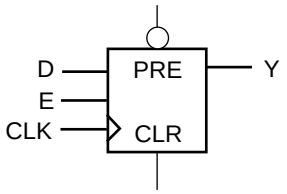



### Module Delays

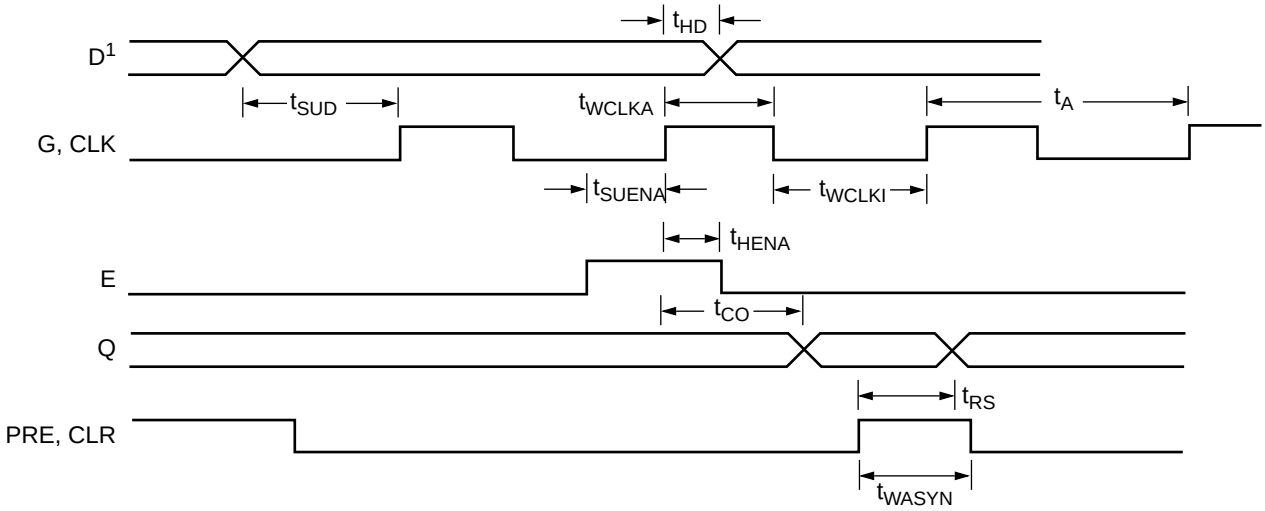


## Sequential Module Timing Characteristics

### Flip-Flops and Latches



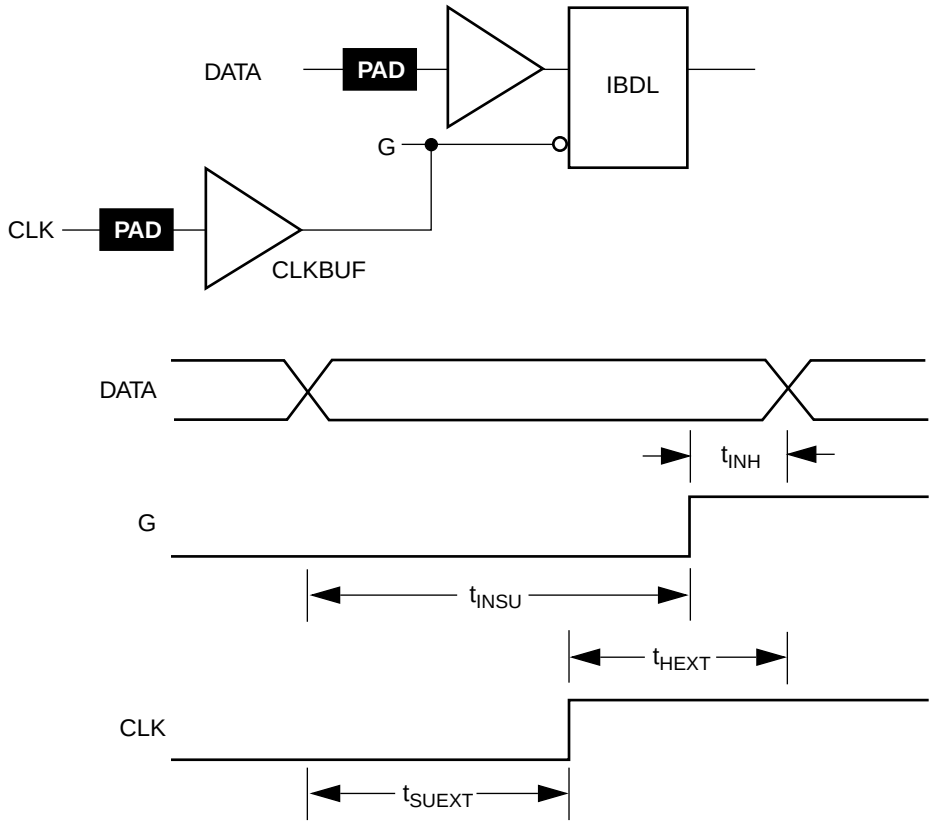

(Positive edge triggered)



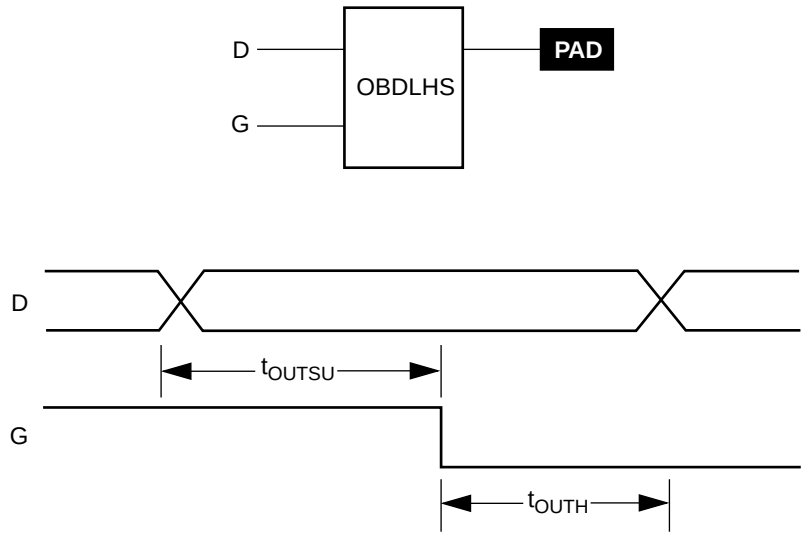

***Note:*** *D represents all data functions involving A, B, and S for multiplexed flip-flops.*

## Sequential Timing Characteristics (continued)

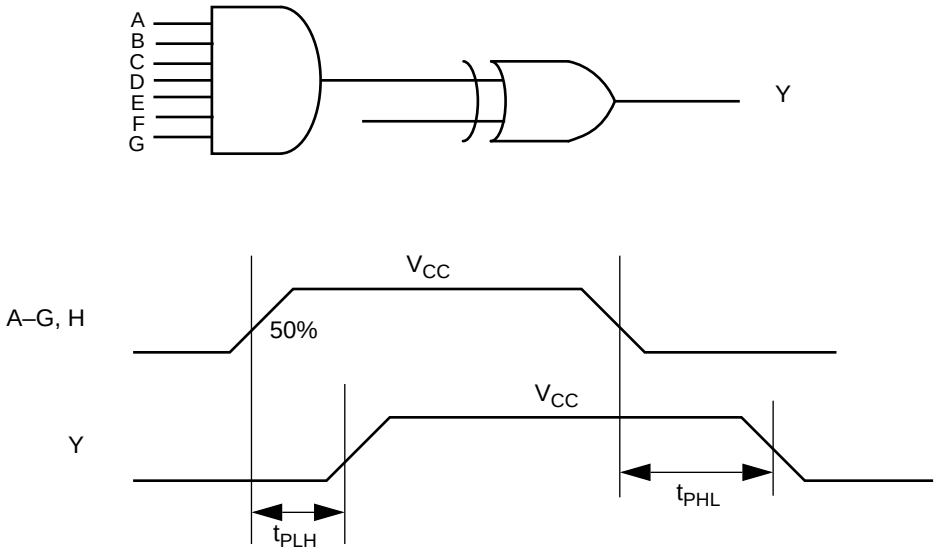
### Input Buffer Latches



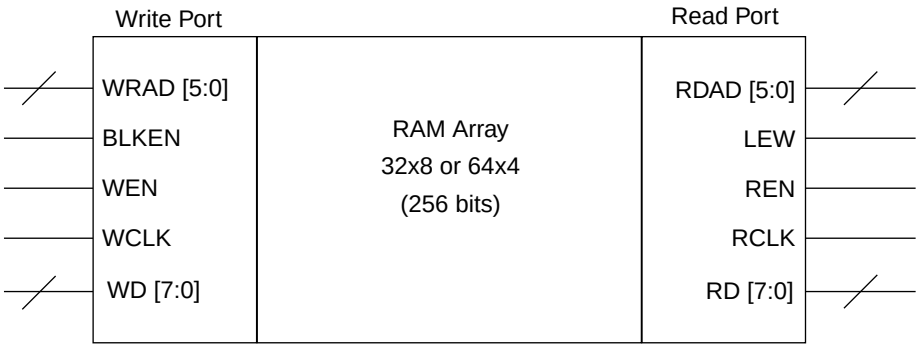

### Output Buffer Latches



## Decode Module Timing

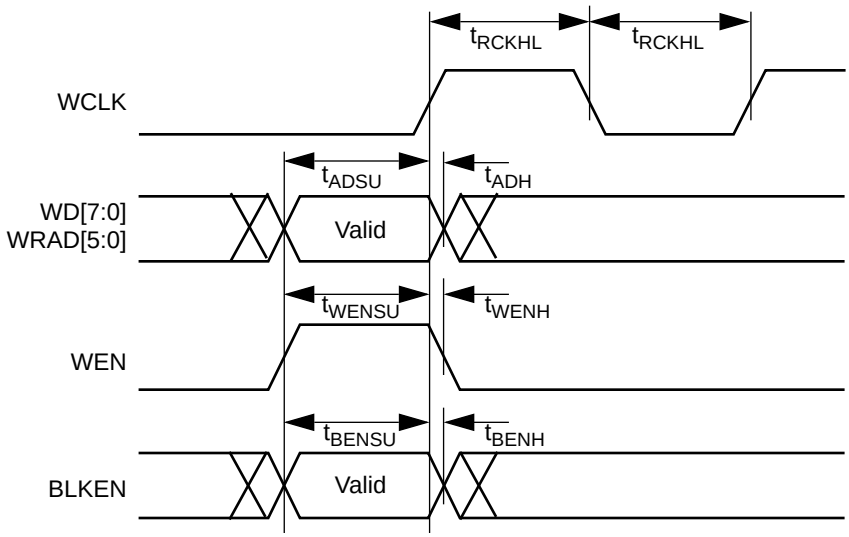



## SRAM Timing Characteristics



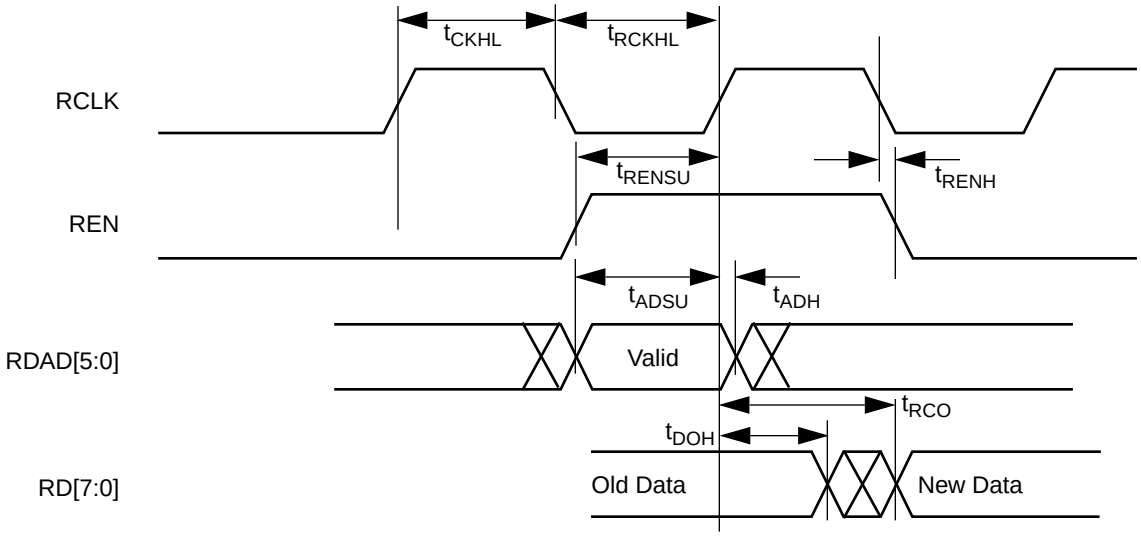
## Dual-Port SRAM Timing Waveforms

### 3200DX SRAM Write Operation




***Note:*** *Identical timing for falling-edge clock.*

### 3200DX SRAM Synchronous Read Operation

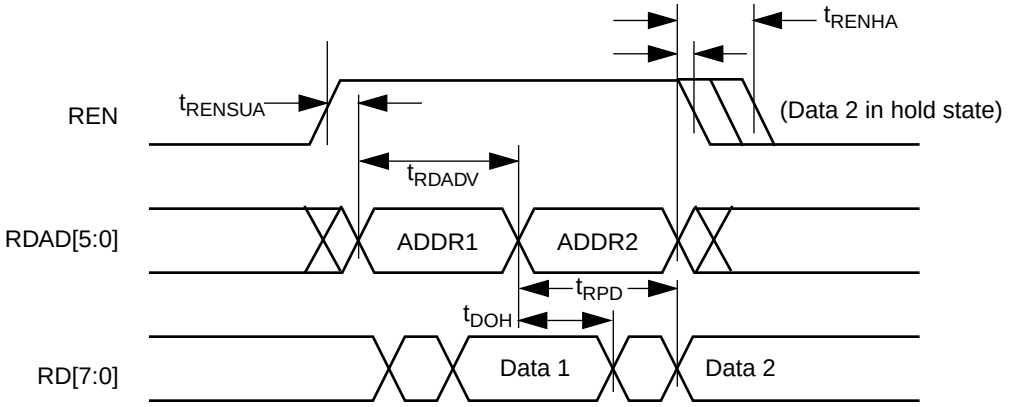



***Note:***

1. *Identical timing for falling-edge clock.*

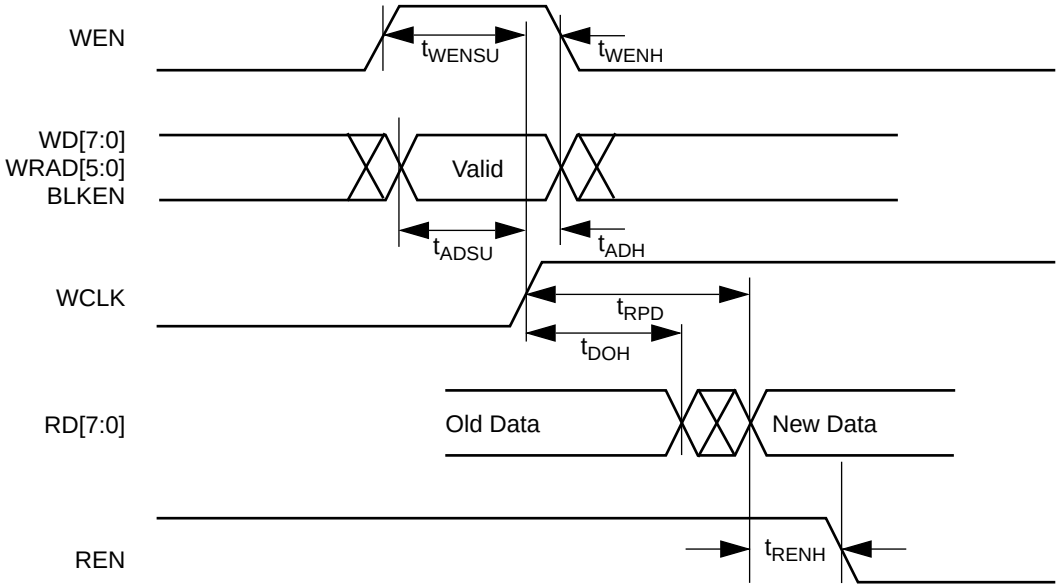
3200DX SRAM Asynchronous Read Operation—Type 1

**(Read Address Controlled)**




32DX SRAM Asynchronous Read Operation—Type 2

**(Write Address Controlled)**



## Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The 3200DX family delivers a very tight fanout delay distribution. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Actel's patented PLICE antifuse offers a very low resistive/capacitive interconnect. The 3200DX family's antifuses, fabricated in 0.6 micron lithography, offer nominal levels of 100 ohms resistance and 7.0 femtofarad (fF) capacitance per antifuse.

The 3200DX fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The 3200DX family's proprietary architecture limits the number of antifuses per path to a maximum of four, with 90% of interconnects using two antifuses.

## Timing Characteristics

Timing characteristics for 3200DX devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all 3200DX family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the ALS Timer utility or performing simulation with post-layout delays.

### Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Since the 3200DX architecture provides deterministic timing and abundant routing resources, Actel's Designer Series development tools offers DirectTime; a timing-driven place and route tool. Using DirectTime, the designer may specify timing-critical nets and system clock frequency. Using these timing specifications, the place and route software optimized the layout of the design to meet the user's specifications.

### Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 3 ns to 6 ns delay. This additional delay is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section.

### Timing Derating

A best case timing derating factor of 0.45 is used to reflect best case processing. Note that this factor is relative to the "standard speed" timing parameters, and must be multiplied by the appropriate voltage and temperature derating factors for a given application.

## Timing Derating Factor (Temperature and Voltage)

| | Industrial | | Military | |
|---|---|---|---|---|
| | **Min.** | **Max.** | **Min.** | **Max.** |
| (Commercial Specification) x | 0.69 | 1.11 | 0.67 | 1.23 |

## Timing Derating Factor for Designs at Typical Temperature ($T_J$ = 25°C) and Voltage (5.0 V)

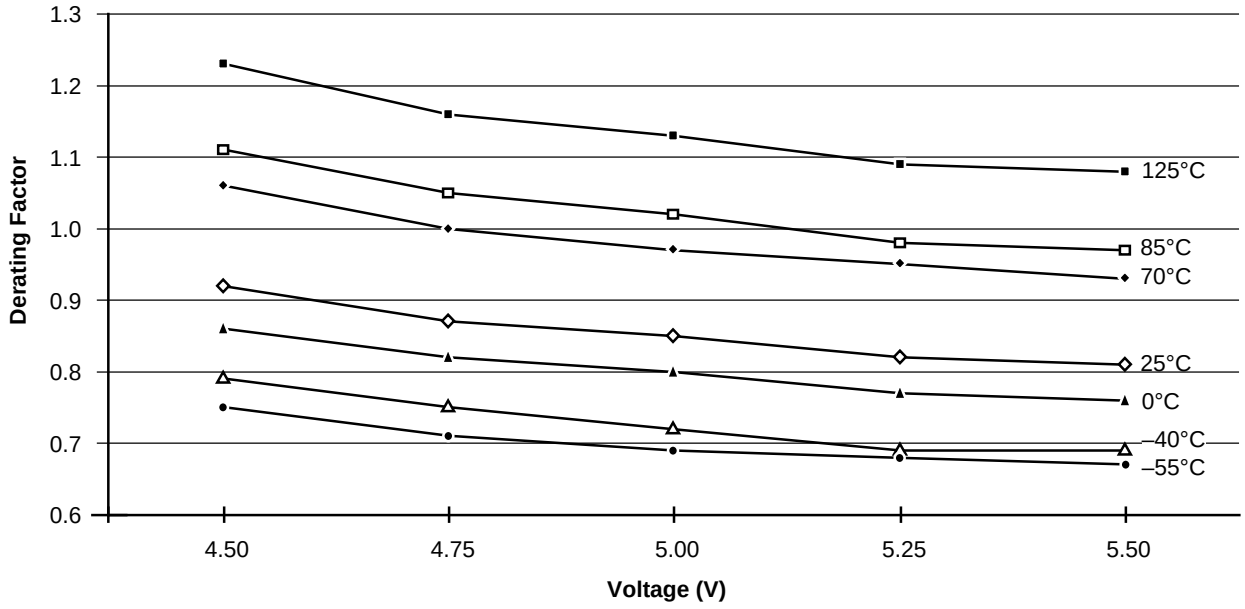
| | |
|---|---|
| (Maximum Specification, Worst-Case Condition) x | 0.85 |

***Note:*** *This derating factor applies to all routing and propagation delays.*

## Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, $T_J$ = 4.75 V, 70°C)

| | –55 | –40 | 0 | 25 | 70 | 85 | 125 |
|---|---|---|---|---|---|---|---|
| **4.50** | 0.75 | 0.79 | 0.86 | 0.92 | 1.06 | 1.11 | 1.23 |
| **4.75** | 0.71 | 0.75 | 0.82 | 0.87 | 1.00 | 1.05 | 1.16 |
| **5.00** | 0.69 | 0.72 | 0.80 | 0.85 | 0.97 | 1.02 | 1.13 |
| **5.25** | 0.68 | 0.69 | 0.77 | 0.82 | 0.95 | 0.98 | 1.09 |
| **5.50** | 0.67 | 0.69 | 0.76 | 0.81 | 0.93 | 0.97 | 1.08 |

**Junction Temperature and Voltage Derating Curves (normalized to Worst-Case Commercial, $T_J$ = 4.75 V, 70°C)**




***Note:*** *This derating factor applies to all routing and propagation delays.*